R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 9 lines 10-19, page 13 lines 2-8, page 2 line 21-page 3 line 3, page 7 lines 14-18 and FIGS. 1 and 3, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 4-15 and 17-20 under 35 U.S.C. §102(a) as being anticipated by Mikawa et al. '673 (hereafter Mikawa) has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Mikawa concerns a logical check apparatus and method for semiconductor circuits and storage medium storing logical check program for semiconductor circuits (Title).

Claim 1 provides a step for automatically generating a repair file based on simulation path data, the repair file predicting at least one of a plurality of fuses to implement a repair to a specific failure of a design. In contrast, column 9 lines 20-32 of Mikawa appear to contemplate a user enters the particular fuses to be blown into the system. Mikawa appears to be

silent regarding an automatic generation of a repair file for a specific failure. Therefore, Mikawa does not appear to disclose or suggest a step for automatically generating a repair file based on simulation path data, the repair file predicting at least one of a plurality of fuses to implement a repair to a specific failure of a design as presently claimed. Claims 12 and 13 provide language similar to claim 1.

Claim 1 further provides a step for generating a repair program **based on the repair file** such that the at least one of the fuses simulates as programmed. In contrast, FIG. 2 of Mikawa appears to show a laser trimming operation command sequence generator 207 of Mikawa generating a laser trimming operation command sequence file 208 **based on the user input selection of a fuse**, instead of a repair file predicting the fuse, to cause the fuse to be "broken" in simulation. The laser trimming fuse element information holder 206 of Mikawa also feeds the laser trimming operation command sequence generator 107 of Mikawa. However, column 7 lines 35-41 of Mikawa appears to suggest that the laser trimming fuse element information holder 206 only holds element identification numbers and "net names connected". Mikawa appears to be silent regarding the holder 206 predicting at least one of the fuses to implement a repair to a specific failure. Therefore, Mikawa does not appear to disclose or suggest a step for generating a repair program based on the repair file such that the at least

one of the fuses simulates as programmed as presently claimed. Claims 12 and 13 provide language similar to claim 1. As such, claims 1, 12 and 13 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides a step for listing an output of the repair program as a list of coordinates for the at least one of the fuses programmed for the repair in terms of a plurality of logical addresses. Despite the assertion in the Office Action, block 221 in FIG. 1, step ST11 in FIG. 2, all of FIG. 5, all of FIG. 6 and the text in column 7 line 61 through column 8 line 7 of Mikawa appear to be silent regarding logical address type coordinates. Therefore, Mikawa does not appear to disclose or suggest a step for listing an output of the repair program as a list of coordinates for the at least one of the fuses programmed for the repair in terms of a plurality of logical addresses as presently claimed. As such, claim 10 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 17 provides a step for checking the repair program for an error in response to the repair failing in the simulation. In contrast, Mikawa appears to be silent regrading checks of programs in response to simulation failures. Therefore, Mikawa does not appear to disclose or suggest a step for checking the repair program for an error in response to the repair failing in the simulation as presently claimed. As such, claim 17 is fully

patentable over the cited reference and the rejection should be withdrawn.

Claims 4, 6, 9, 14, 15 and 18-20 depend from claim 1 or 12, which are now believed to be allowable. As such, claims 4, 6, 9, 14, 15 and 18-20 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 3 and 16 under 35 U.S.C. §103(a) as being unpatentable over Mikawa in view of Sample et al. '967 (hereafter Sample) has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Mikawa concerns a logical check apparatus and method for semiconductor circuits and storage medium storing logical check program for semiconductor circuits (Title). Sample concerns a method and apparatus for design verification using emulation and simulation (Title).

Claim 16 provides a step for mapping a plurality of co-ordinates of the fuses to a plurality of verilog program statements. Despite the assertion in the Office Action, data path item 112 in FIG. 11, and the text in column 1 lines 53-64 of Sample appear to be silent regarding a mapping step between fuse co-ordinates and verilog program statements. Therefore, Mikawa and

Sample, alone or in combination, do not appear to teach or suggest a step for mapping a plurality of co-ordinates of the fuses to a plurality of verilog program statements as presently claimed. As such, claim 16 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2 and 3 depend from claim 1, which is now believed to be allowable. As such, claims 2 and 3 are fully patentable over the cited references and the rejection should be withdrawn.

New claims 21-24 depend from claim 1, which is now believed to be allowable. As such, claims 21-24 are fully patentable over the cited references and should be allowed.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

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